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STRIP MODE SARPROCESSING AT ASK

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'I'he Alaska SAR Facility (AS)') atthe University of Alaska, Fait banks (UAF) is one of several designated Distributed Active Archive Centers (DAAC) in the United States. Since its establishment in 1991, ASI/has been acquiring and processing SAR data from a number of Spaceborne polar orbiting SAR platforms in operations such as European Space Agency's (ESA) ERS- 1/2., and National Space Development Agency (NASDA) of Japan's JERS-1. With the successful laureh of the Canadian Space Agency's (CSA) Radarsat in November of 1995, ASI will be acquiring and processing its SAR data as well.

The processing of strip mode SARdataatASF has been provided by the Alaska SAR Processor (ASP). 'I'he ASP is ahardwatchased processor conceived at the Jet Propulsion Laboratory in 1989 to conduct high speed strip mode SAR processing in support of 1X3-1. It has since been modified to accommodate JERS-1 in 1992, and again for ERS-2 in 1995. It is currently being revised to accept continuous mode data from Radarsat as well. Since its commission to operations at ASF in August of 1991, upward of 120,000 images has been produced On this processor, and to this date, it remains as one of the more reliable high throughput processor, in operations, However, with the advent in modern processing techniques and algorithm that promise higher efficiency and precision, the ASP's once stellar performance is quickly being matched and surpassed. Also, its circa 1989 technology and design is becoming more difficult to operate, and maintain. The future of strip mock processing at ASI is therefore being re-examined; and the idea of designing and implementing a flexible software based precisionstrip mode processor is being put into reality.

This paper provides a historical progression on strip mode SAR data processing capability at ASF. The design ant] implementation of the original ASP will be revisited; as well as the various upgrades and improve] nentsmade over the years to improve its performance and to accommodate new sensors. The requirements, design, and implementation of the next generation ASF strip mode SA R processor, dubbed Precision Processor (PP), will be discussed. Finally, a report on the development status of the ASP as well as the PP will be given,